EXPRESS MAIL NO. EL872099845US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Tae H. Kim Attorney Docket No.: 501299.01

Filed : Concurrently herewith

Title : HYBRID OPEN AND FOLDED DIGIT LINE ARCHITECTURE

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

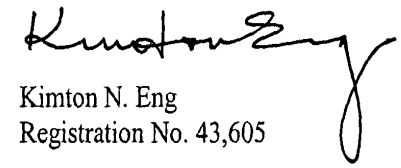
Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicant wishes to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449 (copies of the cited references, as required under 37 C.F.R. § 1.98, are enclosed). Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicant's duty to disclose all information he is aware of which is believed relevant to the examination of the above-identified application, applicant believes that his invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

DORSEY & WHITNEY LLP



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Enclosures:
Form PTO-1449
Cited References (2)

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FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 501299.01	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Tae H. Kim	
		FILING DATE Concurrently herewith	GROUP ART UNIT Not Yet Assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AK							
	AL							
	AM							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AN	Kirihata, T. et al., "A 113mm^2 600Mb/s/pin 512Mb DDR2 SDRAM with Vertically-Folded Bitline Architecture", IEEE International Solid State Circuits Conference, February 2001, pp. 382-383 and 468.
	AO	Yoon, H. et al., "A 4Gb DDR SDRAM with Gain-Controlled Pre-Sensing and Reference Bitline Calibration Schemes in the Twisted Open Bitline Architecture", IEEE International Solid-State Circuits Conference, February 2001, pp. 378-379 and 467.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).